TAXI DAQ Board

an Option for the Surface Detector(?)

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HELMHOLTZ ASSOCIATION

DESY

TAXI Overview

- Transportable Array for eXtremely large area Instrumentation studies
- Environmentally robust air shower test array
- For more information: T. Karg et al., arXiv:1410:4685 [astro-ph.IM]
- Uses segmented plastic scintillators as air shower trigger and reference
- **The TAXI readout board could also be interesting for a surface array at South Pole!**

Design Goal for Scintillation Detector Readout

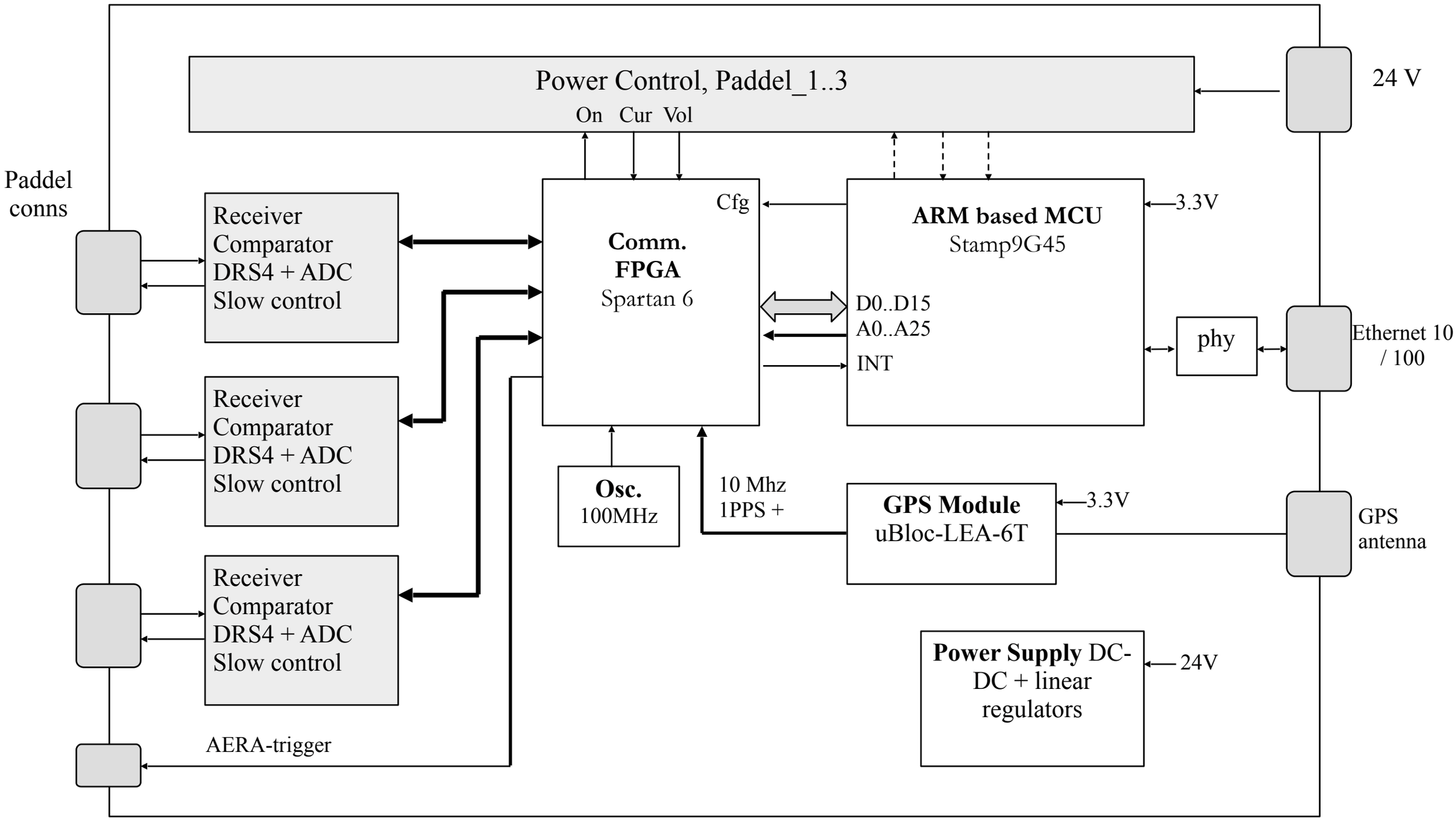
- 24 analog channels with differential input
- 24 discriminators with programmable threshold
  - minimum detectable signal: 1 mV_{pk}
- TDC functionality, time diff. measurements with 0.5 ns accuracy
- Time stamping
- Communication via ethernet 10/100

Can plug into Field-DOMHub

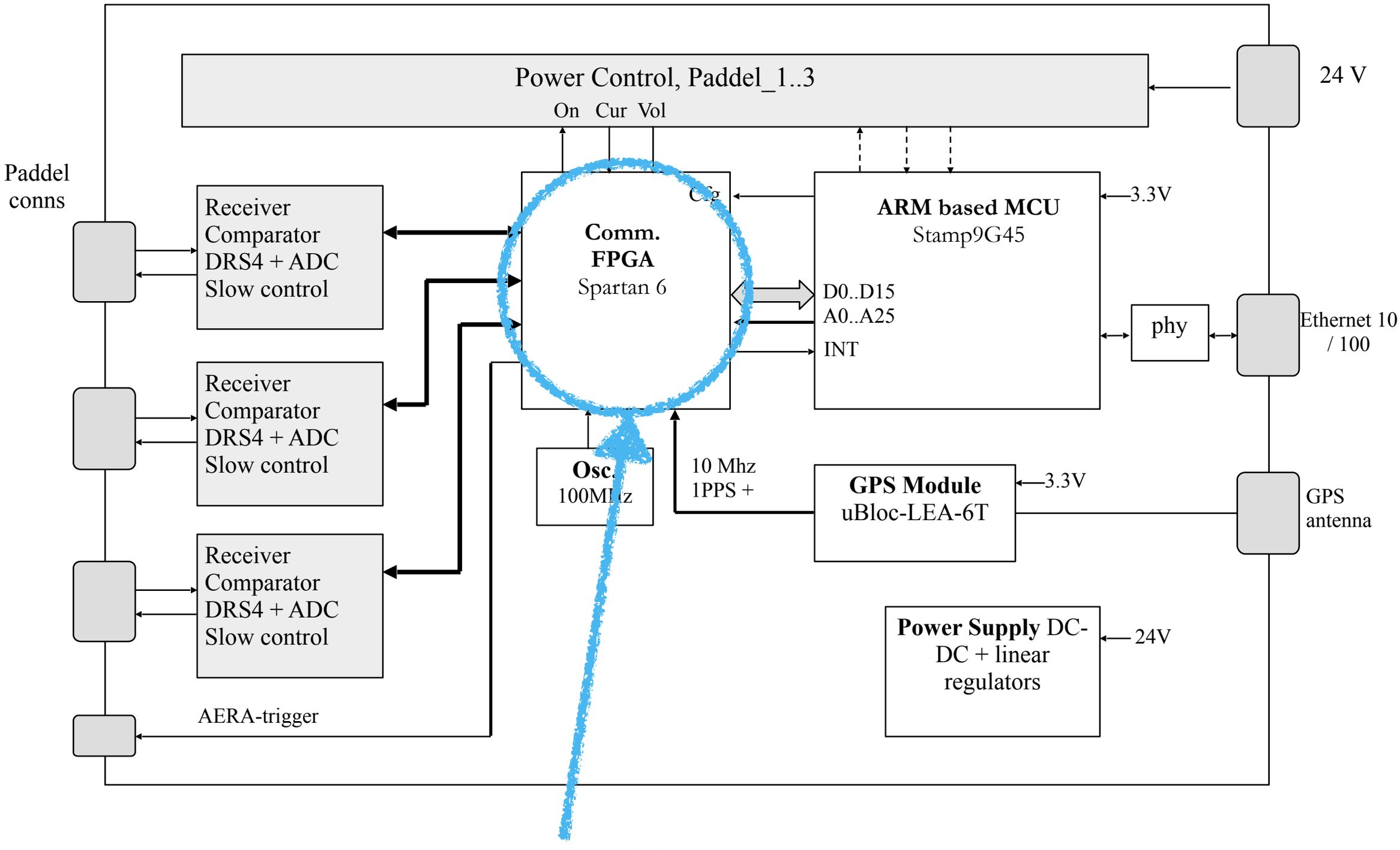
- Single board design, power consumption < 10 W (w/o ADC)
- Single low cost Xilinx FPGA, Spartan 6
- Optional 24 ADC channel, 1024 samples per channel
  - Sampling rate 200 MSPS … 6 GSPS (DRS4)
  - Dead time: TBD

DESY

TAXI Station



TAXI Station



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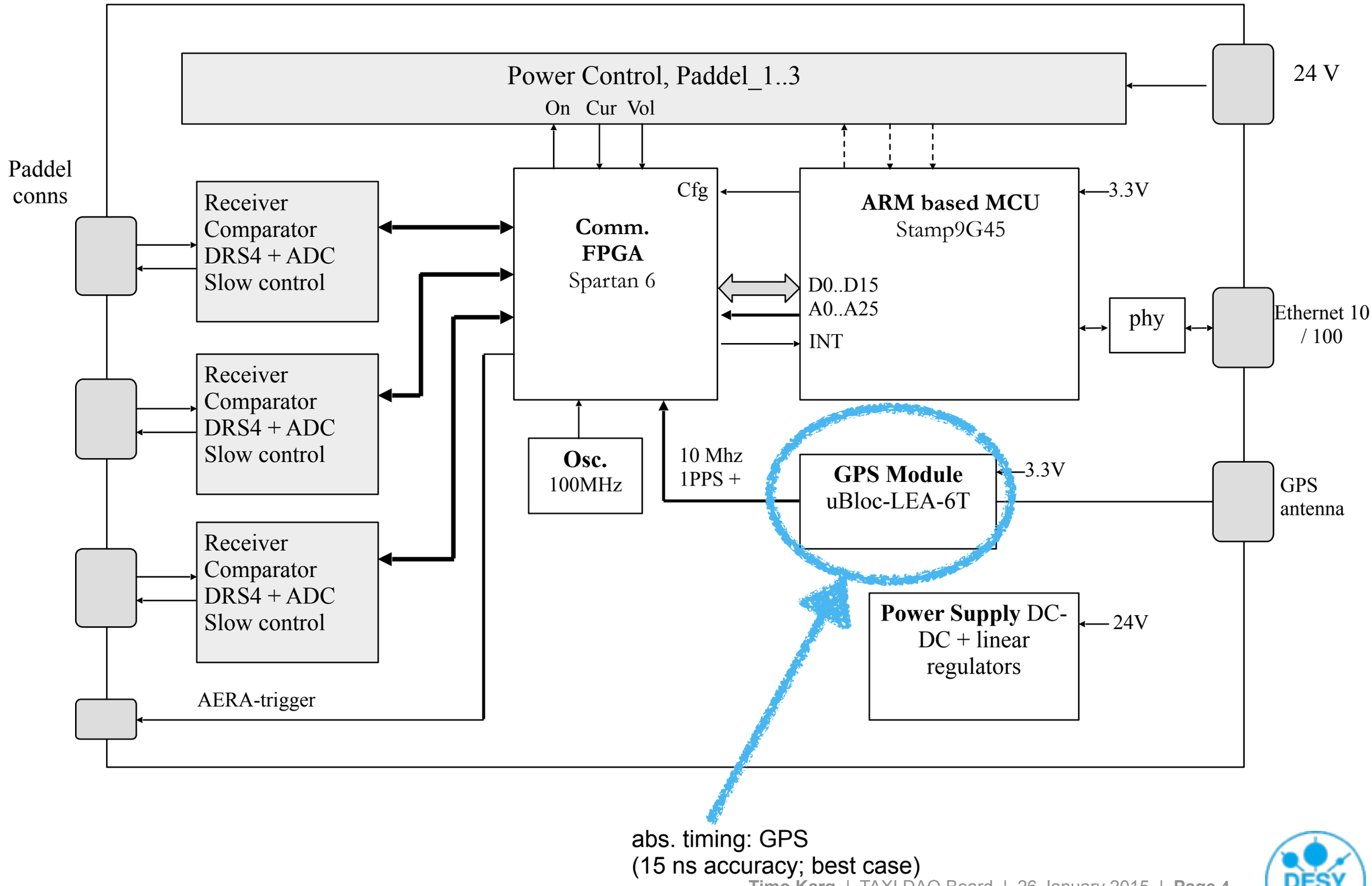

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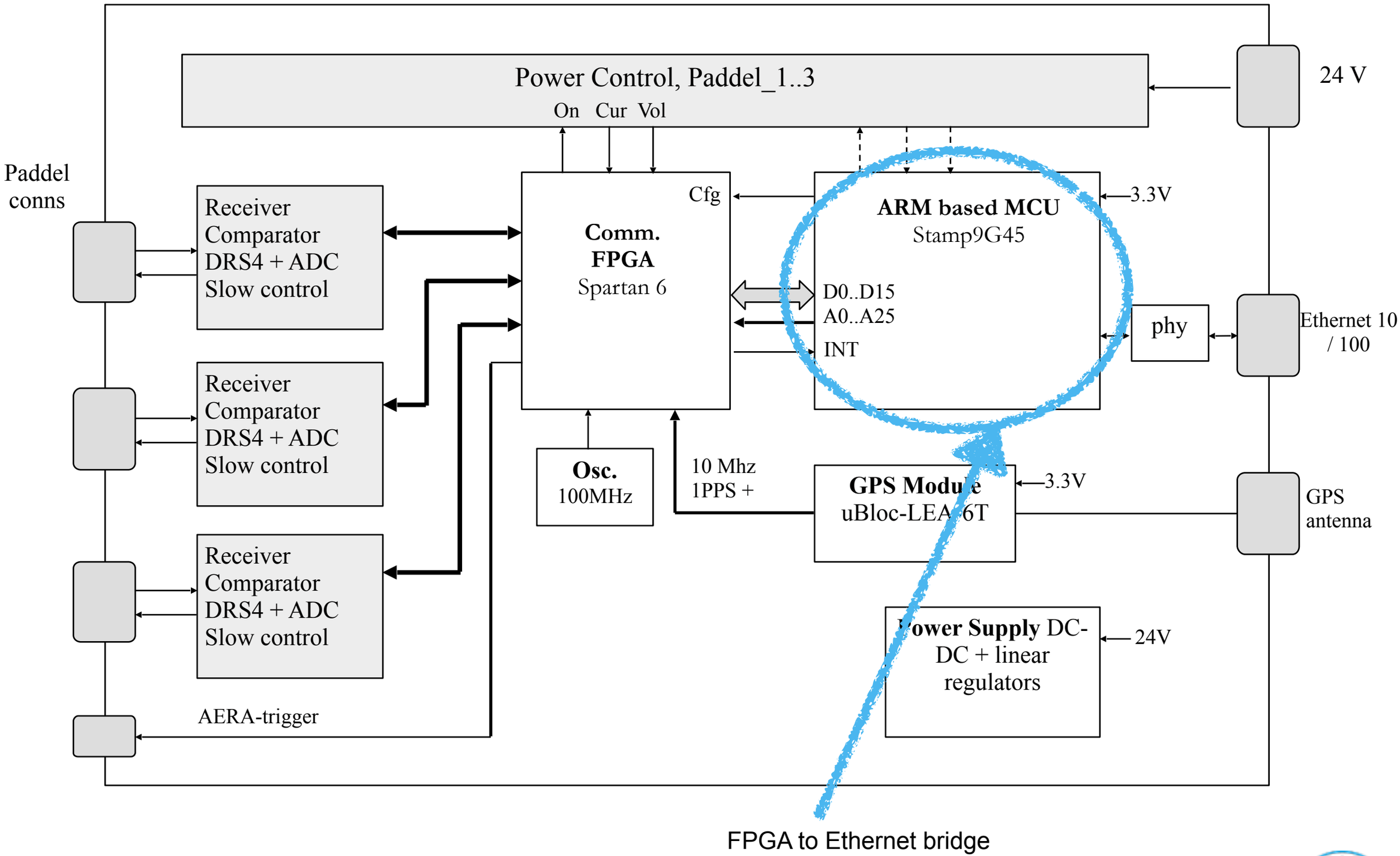

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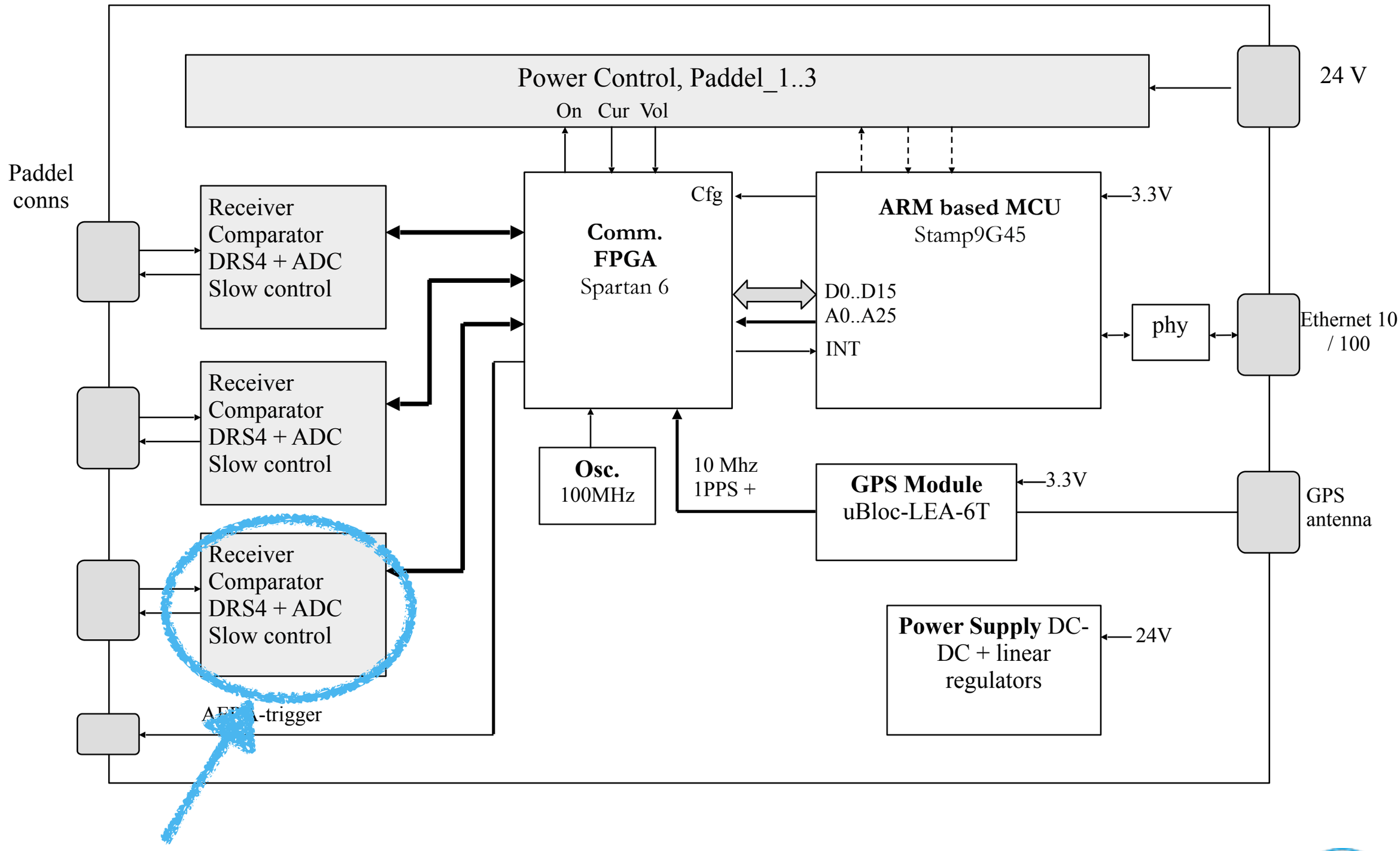


optional, switchable
ring sampler
(waveforms for calibration, debugging)

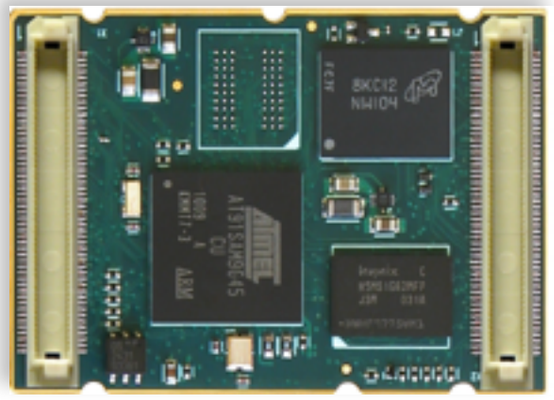
Status and Timeline

- PCB layout finished
- PCB production until mid-February
- All electronics components purchased
  - will be mounted by DESY workshop
- 1st prototype expected in March
- Commissioning and testing

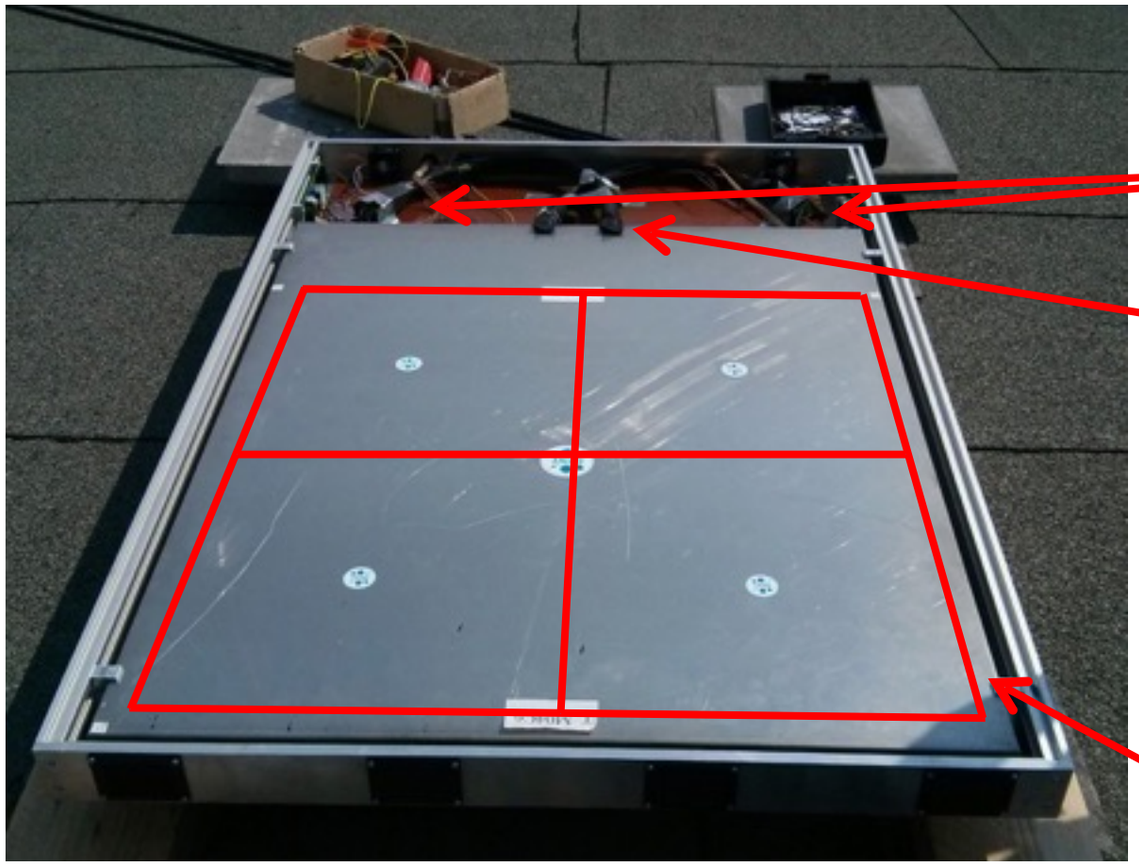
Backup Slides

Ethernet to FPGA Bridge

- ARM based MCU unit (100 €), primarily as ethernet to comm. FPGA bridge
  - Stamp9G45's PCB is only 53.6x38x6.0 mm
  - AT91SAM9G45 runs at 400 MHz with a memory bus frequency of 132 MHz
  - 10/100 Mbit Ethernet, USB, UARTs, …
  - 128 MB NAND flash memory (optional up to 1GB)
  - 128 MB LPDDR-SDRAM (optional up to 512 MB)
  - 16-Bit parallel CPU-Bus (fast FPGA conn.)
  - Memory mapping, DMA, …
  - See also http://www.taskit.de/home.html
  - Comes with real time linux development system
  - Widely used at DESY Zeuthen
  - 400 MHz ARM core can do more than just moving data
  - Might be replaced later
    - e.g by adding the interface part to the Xilinx FPGA



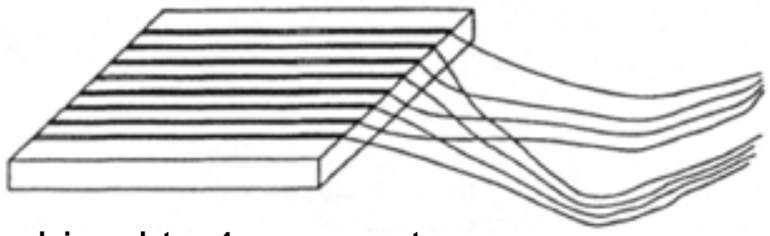
Scintillation Detector



Hamamatsu R 5900-3-M4
2 × 2 multi-anode PMT

optical fibers
each tile read out by 2 sets of fibers

1 m^2 tiled plastic scintillator
16 tiles, 25 × 25 cm each



combined to 4 segments
of 50 × 50 cm for readout

- Input: ± 12 V
- Output: differential,
  analog PMT signal (8 channels)